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A NEW THREE PHASE SINGLE STAGE RECTIFIER

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ABSTRACT

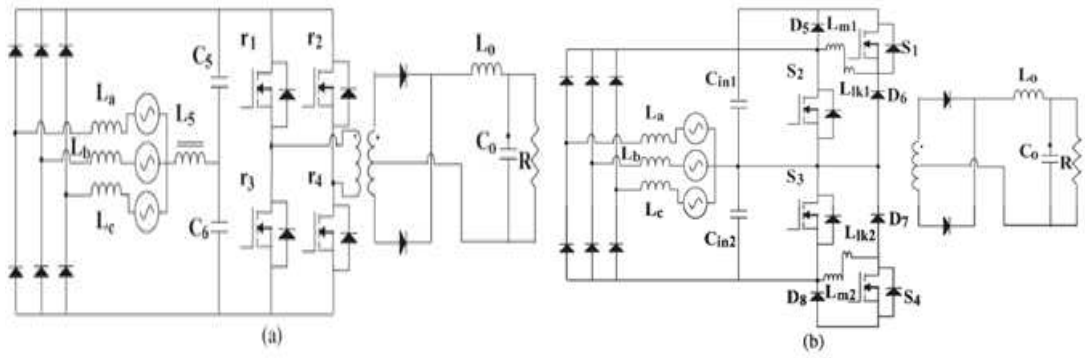
A new three-phase single-stage rectifier is proposed in this paper. The features of the proposed rectifier are that produce input currents that does not have dead time regions and an output current that can be continuous when the converter is operating from maximum load to at least half of the load. In this paper, the operation of the new converter is explained, its features and design are discussed in results, and its operation is confirmed with experimental results obtained from a prototype.

KEYWORDS: AC–DC Power Conversion, Single-Stage Powerfactor Correction (SSPFC), Three-Level Converters, Three-Phase

I. INTRODUCTION

This approach, however, is expensive and complicated as it needs ten active switches along with associated gate drive and control circuitry. Moreover, the converter must be operated with sophisticated control methods that require the converters. Proposed alternatives have included: 1) using three separate ac-dc boost converter modules [2]; 2) using a reduced switch ac-dc converter [3]; and 3) using a single-switch boost converter [4]. Two separate switch-mode converters are still needed, however, to perform three-phase ac-dc power conversion with transformer isolation.

Researchers have tried to further reduce the cost and complexity associated with single-phase [5]–[12] and three-phase [13]–[24] ac-dc power conversion and PFC by proposing single-stage converters that integrate the functions of PFC and isolated dc-dc conversion in a single power converter. Several examples of three-phase single-stage converters are shown in Figure 1. Previously proposed three-phase single-stage ac-dc con- verters, however, have at least one of the following drawbacks that have limited their widespread use.



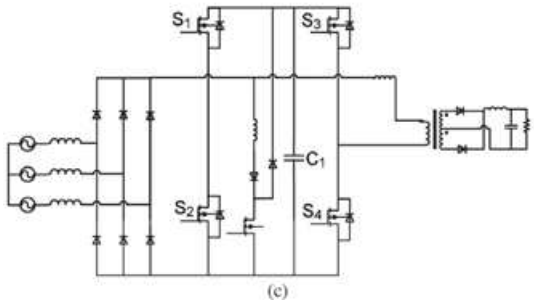


Figure 1: Three-Phase Single-Stage Ac-Dc Converters. (a) Three-Phase Reduced Switch ac-dc Converter [16]. (b) [17]. (c) [18]

- Input currents are distorted and contain a significant amount of low-frequency harmonics because the converter has difficulty performing PFC and dc-dc conversion simultaneously [16].

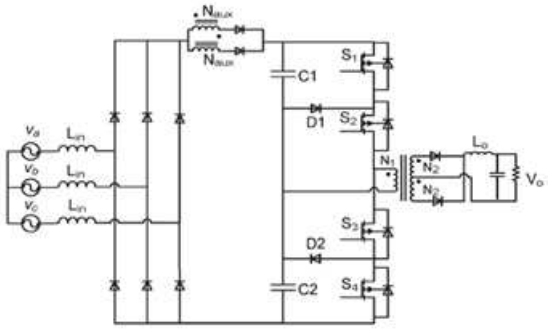


Figure 2: Proposed Converter

- Converter must be controlled using very sophisticated techniques and/or nonstandard techniques [5]–[11]. This is particularly of resonant type converter that need variable switching frequency control methods to operate. 5) Output inductor must be very low, which makes the output current to be discontinuous. This paper presents a new three-phase, single-stage rectifier that does not have any of these drawbacks. In this paper, the operation of the new converter is explained, its features and design are discussed in results, and its operation is confirmed with experimental results obtained from a prototype.

II. CONVERTER OPERATION

The converter transformer to cancel the dc bus capacitor voltage so that the voltage that appears across the diode bridge output is zero. This voltage cancellation occurs whenever there is voltage across the main transformer winding and current in the input inductors rises when it does. When there is no voltage across the main transformer primary winding, the total voltage across the dc bus capacitors appears at the output of the diode bridge; since this voltage is greater than the input voltage, the input currents falls. If the input currents are discontinuous, they will be naturally nearly sinusoidal (when filtered) and in phase with the input voltages. To simplify the analysis, the following assumptions are made: 1) The input voltage value can be considered as constant within a switching period as the period of the three-phase voltage supply is much longer than the switching period; 2) All devices are ideal; 3) The currents in inductors *La* = *Lb* = *Lc* = *L*in are *iLa*, *iLb*, *iLc* and have the same amplitude; 4) The dc bus voltage has no ripple.

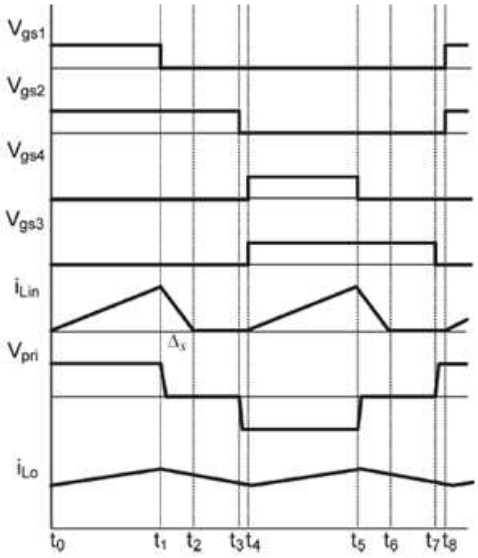


Figure 3: Typical Waveforms Describing the Modes of Operation

The equivalent circuit in each stage is shown in Figure 4. The converter goes through the following modes of operation in a half switching cycle.

Due to magnetic coupling, a voltage appears across one of the auxiliary windings and cancels the total dc bus capacitor voltage; the voltage at the diode bridge output is zero, and the input currents rise. Due to the high switching frequency, the supply voltage is assumed constant within a switching cycle. In this mode, the three-phase input current equations are as follows:

$$v_a = L_a \frac{di_{L_a}}{dt}$$

$$v_b = L_b \frac{di_{L_b}}{dt}$$

$$v_c = L_c \frac{di_{L_c}}{dt} \ldots\ldots\ldots\ldots \quad \ldots\ldots (1)$$

$$i_{L_a} + i_{L_b} + i_{L_c} = 0$$

$$v_a + v_b + v_c = 0$$

As it can be seen from (1), the equations that describe the relation between the current and voltage of input currents *iLa*, *iLb*, and *iLc are* the same, but with different notation. Therefore, instead of using terms with subscripts a, b, and c in this paper, a general notation → is defined so that only one equation is written instead of three equations. Equation (1) can thus be rewritten as,

$$\vec{v} = L_{in} \frac{d\vec{i}_{L_{in}}}{dt} \ldots\ldots\ldots\ldots \quad \ldots.(2)$$

The auxiliary inductor current increases during this mode, and the following expression can be written:

$$\overrightarrow{i_{L_{in,k}}(k)} = \frac{|\overrightarrow{v_k}|}{L_{in}} . t \ldots\ldots\ldots\ldots\ldots \quad \ldots\ldots(3)$$

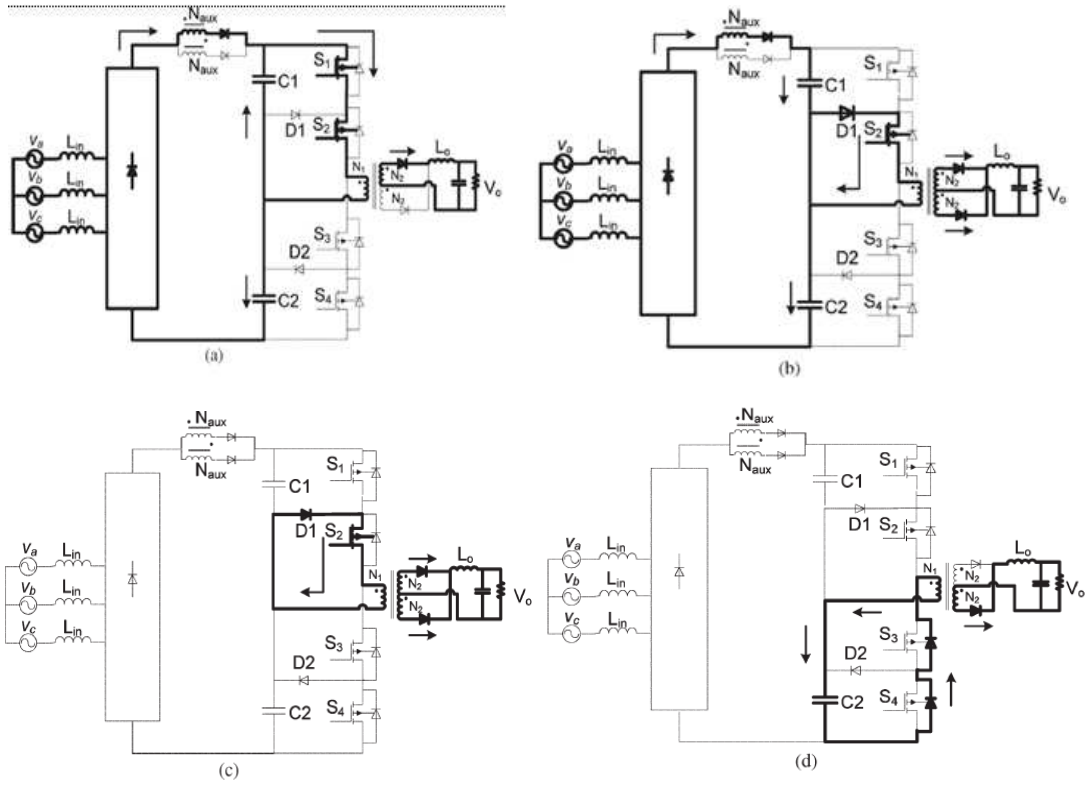


Figure 4: Modes of Operation. (a) Mode 1 (*t*0 < *t* < *t*1). (b) Mode 2 (*t*1 < *t* < *t*2). (c) Mode 3 (*t*2 < *t* < *t*3). (d) Mode 4 (*t*3 < *t* < *t*4)

At the end of Mode I, the current in the auxiliary inductor *L*in, during the kth interval is

$$\vec{i}_{L_{in},k,max} = \frac{|\overrightarrow{v_k}|}{L_{in}} . \frac{D}{2f_{sw}} \ldots\ldots\ldots\ldots \quad \ldots. (4)$$

Where *vk* is the average value of the supply voltage in the interval k, D is the duty cycle, and *fsw* is the switching frequency. Since the converter operates with a steady-state duty cycle D that is constant throughout the line cycle, the peak value of an input inductor current at the end of this mode is dependent only on the supply voltage.

The output inductor current can be expressed as

$$i_{L_o}(t) = \frac{\frac{v_{bus}}{2N} - v_L}{L_o} . t \ldots\ldots\ldots\ldots\ldots \quad \ldots.(5)$$

If it is assumed that the output inductor current is continuous, then the following expression for peakto- peak ripple can be derived:

$$\Delta i_{L_o} = \frac{v_{bus} - v_L}{L_o} . \frac{D}{2f_{sw}} \ldots\ldots\ldots \quad \ldots\ldots\ldots(6)$$

Mode 2 (*t*1 < *t* < *t*2) *[Figure. 4(b)]:* In this mode, *S*1 is OFF, and *S*2 remains ON. The energy stored in the auxiliary inductor during the previous mode is completely transferred into the dclink capacitor. The amount of stored energy in the auxiliary inductor depends upon the rectified supply voltage. This mode ends when the auxiliary inductor current reaches zero. Also, during this mode, the load inductor current freewheels in the secondary of the transformer. The voltage across the auxiliary inductors in Mode II is $|-\rightarrow Vk| - V$bus, thus, the auxiliary current expression is as follows:

$$\frac{d\vec{i}_{L_{in}}}{dt} = \frac{|\vec{v_k}| - v_{bus}}{L_{in}}$$

$$\vec{i}_{L_{in},k}(t) = i_{L_{in},k}, max - \frac{v_{bus} - |\vec{v_k}|}{L_{in}}.t \ldots\ldots \quad (7)$$

This mode ends when the auxiliary inductor current reaches zero. This mode lasts for $\Delta s,k/2fsw$ amount of time; using (4), the following expression can be found:

$$\vec{\Delta_s}, k = \frac{|\vec{v_k}|}{v_{bus} - |\vec{v_k}|} D \ldots\ldots\ldots\ldots \quad \ldots..(8)$$

Where $\Delta s,k$ is the normalized period of Mode II. Equation (8) shows that the duration of this mode is time varying along one ac line period. In order to ensure a discontinuous input current, the normalized period $\Delta s,k$ must satisfy the expression $D+\Delta s,k < 1$ for any interval k and any load conditions. Using (8), this constraint can be written as

$$v_{bus} > \frac{|\vec{v_k}|}{1-D} \ldots\ldots\ldots\ldots\ldots\ldots \quad \ldots.(9)$$

On the other hand, the load inductor current freewheels in the secondary of the transformer, which defines a voltage across the load filter inductor equal to $-VL$; therefore, the load inductor current is given by

$$i_{L_o}(t) = i_{L_o,max} - \frac{v_L}{L_o} t \ldots\ldots\ldots \quad \ldots.(10)$$

$$\Delta i_{L_o} = \frac{v_L}{L_o} \quad \frac{1-D}{2f_{sw}} \ldots\ldots\ldots\ldots \quad \ldots\ldots..(11)$$

Consequently, the following expression can be derived from (6) and (11)

$$v_o = \frac{v_{bus}}{2N} D \ldots\ldots\ldots \quad \ldots\ldots\ldots\ldots..(12)$$

There is no energy transferred to the dc bus capacitors. *Mode 4* ($t3 < t < t4$) *[Figure 4(d)]:*. For the remainder of the switching cycle, the converter goes through Modes 1 to 4, but with *S*3 and *S*4 ON instead of *S*1 and *S*2. The rectified supply voltage of each phase, and the current flowing through each inductor increases.

Mode 6 ($t5 < t < t6$)*:* In this mode, *S*3 is ON, and *S*4 is OFF. The energy stored in the auxiliary inductors during the previous mode is completely transferred into the dc-link capacitor.

Mode 7 ($t6 < t < t7$)*:* In this mode, *S*4 is OFF, and the primary current of the main transformer circulates through the diode *D*2 and *S*3. The output inductor current also freewheels in the secondary of the transformer during this mode.

Mode 8 ($t7 < t < t8$)*:* In this mode, *S*3 and *S*4 are OFF, and the primary current of the transformer charges the capacitor *C*1 through the body diodes of *S*1 and *S*2. Switches *S*1 and *S*2 are switched on at the end of this mode.

Output voltage regulation can be done by standard control methods that control duty cycle D. Duty cycle, D in (4), is defined as the time when *S*1 and *S*2 are both ON during the first half cycle or when *S*3 and *S*4 are both ON during the second half cycle. These two cases correspond to energy transfermodes of operation. Any control method that can be used to regulate a two-level full-bridge converter by controlling D can be used to regulate the proposed converter; the only difference is how the gating signals are implemented. For example, the control for the proposed converter can be implemented with a conventional phase-shift PWM controller, and some logic can be added to the output of the controller to generate the appropriate gating signals.

Various such techniques have been proposed in the literature, including techniques that sense the capacitor voltages and adjust the duty cycle of the converter switches appropriately. For this work, an auxiliary circuit that consists of a transformer with a turns ratio of *N*aux1/*N*aux2 = 1 and two diodes *D*aux1 and *D*aux2 was used, as now shown in Figure 5(a) [25]. This circuit is very simple, small, and handles only a small fraction of the overall power that is processed by the converter so that the low current rated diodes can be used (<1 A) and a small core can be used for the transformer. It should be noted that the auxiliary circuit can take care of the voltage balancing, which allows a standard controller to be used for the full bridge.

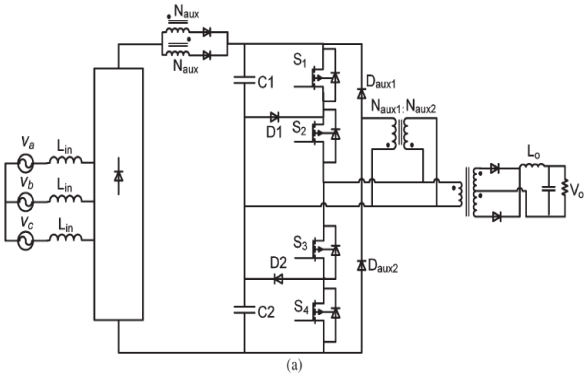
The basic principle behind the auxiliary circuit is that if the voltage across one capacitor begins to be greater than the other by more than a diode drop, then one of the diodes begins to conduct as energy is transferred away from the capacitor with the higher voltage. Since the auxiliary circuit does not allow for large differences in bus capacitor voltage, the amount of energy that needs to be transferred away at any given time is small. When the auxiliary circuit is added to the main circuit, it is most likely to come into play during Modes 1 and 5 of operation as this is when the most current will flow through one of the bus capacitors. The auxiliary circuit works as follows during these modes.

Mode 1 ($t0 < t < t1$) *[Figure 5(b)]:* During this mode, switches *S*1 and *S*2 are ON, and energy from the dc-link capacitor *C*1 flows to the output load. Since the auxiliary winding generates a voltage that is equal to the total dc-link capacitor voltage (sum of *C*1 and *C*2), the voltage across the auxiliary inductor is the rectified supply voltage. This allows energy to flow from the ac mains into the auxiliary inductor during this mode, and the auxiliary inductor current increases.

At the beginning of this interval, if there exists any unbalance between the voltages of the two dc-bus capacitors, such that *VC*1 > *VC*2, the auxiliary circuit starts conducting through diode *D*aux2 to balance the voltage difference across the *C*1 and *C*2. To balance the voltage difference across the capacitors.

III. STEADY-STATE ANALYSIS

In order to develop a procedure that can be used to design the proposed converter, the steady-state operation of the converter must be analyzed to determine its behavior for any given set of specifications (line-to-line input voltage *Vll*, rms, output voltage *Vo*, output current *Io*, and switching frequency *fsw*) and any given set of component values input inductors *La* = *Lb* =*Lc* = *L*in, duty ratio D, transformer turns ratio *N* = *n*1/*n*2, output inductor *Lo*). Important converter characteristics can be determined after the analysis has been performed and then used to develop the design procedure.



(a)

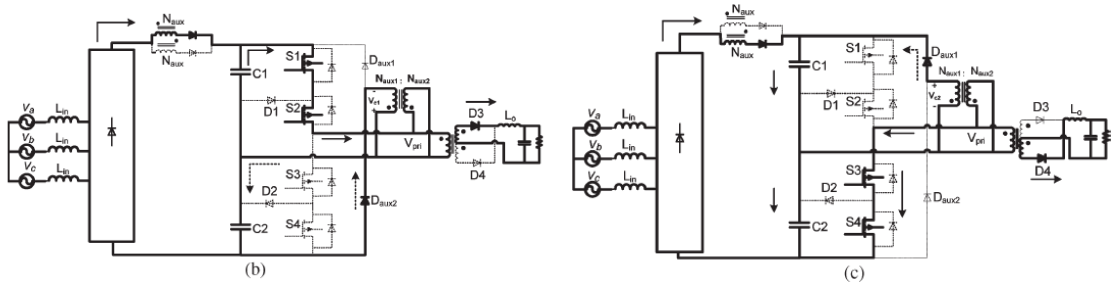


Figure 5: (a) Proposed Single-Stage Three-Level Converter with Auxiliary Circuit (b) Mode 1 with Auxiliary Circuit (c) Mode 5 with auxiliary circuit.

Such as input current can be determined. Unlike a conventional two-stage converter, a single-stage converter is not solely regulated by the ac-dc boost PFC stage and cannot be purposefully kept constant. This voltage can be derived by noting that energy equilibrium must exist for storage capacitor when the converter is in steady-state operation.

The energy pumped into the capacitor from the input section must be equal to the energy that provides to the output, so that the net dc current flowing in and out of must be zero during a half-line cycle. However, this cannot be determined by an equation with a closed-form solution due to the various possible combinations of input and output modes of operation, but must instead be determined using a computer program.

Magnetizing current, then for an operating point with given input voltage *V*in, output voltage *VL*, switching frequency *fsw*, input inductor *L*in, output inductor *Lo*, transformer turns ratio *N* = *N*pri/*N*sec, and output current *Io* can be determined as follows:

1) Select the set of specifications and components values to be considered. Assume a duty cycle D as an initial "guess"; (i.e., *D* = 0.5) to start the process of determining a corresponding dc bus capacitor voltage *V*bus.
2) Assume that the output current is continuous; then, use (12) to find *V*bus

$$v_{bus} = \frac{2v_o N}{D} \ldots\ldots\ldots \qquad \ldots\ldots\ldots\ldots(13)$$

3) With this value of V_{bus}, verify that the output current is continuous by seeing that the peak output current ripple does not exceed the average current I_0

$$\frac{1}{2}\frac{\frac{v_{bus}}{2N}-v_o}{L_o}.\frac{D}{2f_{sw}} < I_o \ldots\ldots \qquad \ldots\ldots\ldots..(14)$$

If this relation is satisfied, then *V*bus is equal to the value determined in (13). If not, then the output current is discontinuous and V_{bus} must be determined using (15), which has been derived for discontinuous current mode (DCM)

$$v_{bus} = 2N\frac{v_o-\sqrt{{v_o}^2+\frac{16p_oL_of_{sw}}{D^2}}}{2}\ldots \qquad \ldots(15)$$

4) With *V*bus known, find the average current that flows out of capacitors during a half-line cycle using either (16) for continuous current mode (CCM) or (17) for DCM

$$I_{cb,out-avg} = \frac{I_o D}{2N}\ldots\ldots\ldots \qquad \ldots\ldots\ldots \ldots(16)$$

$$I_{cb,out-avg} = \frac{D^2}{4NL_of_{sw}}\left(\frac{v_{bus}}{2N}-v_o\right)\ldots \qquad (17)$$

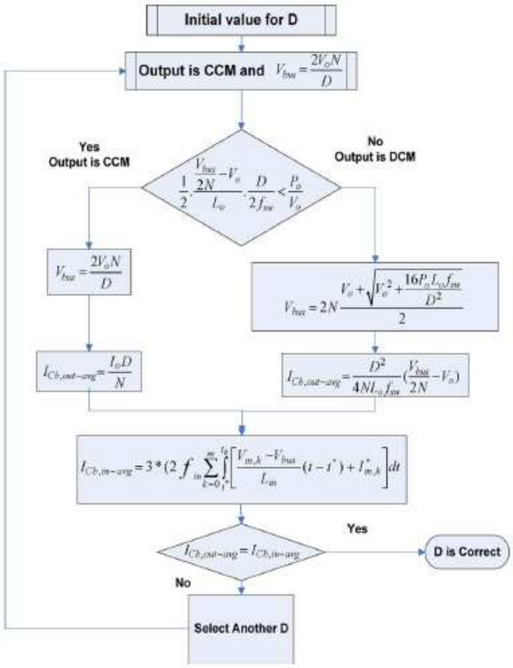


Figure 6: Procedure of Steady-State Analysis for Determining the Dc Bus Voltage

5) Determine the average current that is fed from the input to capacitors during a half-line cycle using (17)

$$I_{cb,in-avg} = 3 * \left(2f_{in} \sum_{k=0}^{m} \int_{t^*}^{t_k} \left[\frac{v_{in,k} - v_{bus}}{L_{in}}(t - t^*) + I_{in,k}{}^*\right] dt\right) \ldots\ldots\ldots \quad (18)$$

Where I*in,k is the peak input current value during a switching cycle k. If (18) is equal to (14) or (15), then the converter is confirmed to be operating under steady-state conditions, and the value of *V*bus that has been calculated is valid. If not, then the operating point for which is to be determined is not a valid operating point, and the procedure must be repeated for a different value of D. The flowchart in Figure 6 shows the procedure for the steady-state analysis, which can be implemented in a computer program.

IV. CONVERTER CHARACTERISTICS

The procedure discussed in Section III can be repeated to determine *V*bus (or any other parameter) for other operating points, in order for curves to be generated for analysis and design purposes. The converter operating characteristics for any given input and output voltage are dependent on three key parameters: transformer turns ratio N, input inductance *L*aux, and output *Lo*. In this section, the effect of each of these parameters is examined with graphs of characteristic curves that have been generated with a computer program based on the procedure described above.

A. Effect of Output Inductor Value Lo on DC Bus Voltage Vbus

It can be seen from Figure 7(a) that varying *Lo* (but keeping all the other parameters fixed) has a slight effect on *V*bus for higher output loads when the output is operating in CCM, but does so at lower output loads when the output is in DCM. This is because more energy can be transferred from the dc bus capacitor to the output when the output inductor current is discontinuous rather than continuous, for the same amount of average output current.

B. Effect of Input Inductor Value Lin on DC Bus Voltage Vbus

Similar to what was stated above for the output inductor, less energy is transferred from the input to the dc bus when the inductor is larger and the current is more likely to approach the boundary of CCM and DCM.

C. Effect of Transformer Turns Ratio N on DC Bus Voltage

Pump out so much energy that the energy equilibrium at capacitor will result in a very low dc bus voltage that will in turn force the converter to operate with an output voltage that will always be lower than the required value, particularly under heavy load conditions. Likewise, if *N* is very high, then *C*1 and *C*2 may pump out so little energy that that the energy equilibrium *C*1 and *C*2 will result in a very high dc bus voltage that will in turn force the converter to operate with an output voltage that will always be higher than the required value, particularly under light load conditions.

D. Effect of Input Voltage Vin on DC Bus Voltage Vbus

Figure 7(d) shows the effect of input voltage on dc bus voltage. As can be seen, increasing the input voltage increases the dc bus voltage. This is because more energy is pumped into the capacitors when the input voltage is at high line

V. CONVERTER DESIGN

A procedure for the design of the converter is presented in this section and is demonstrated with an example. The following criteria should be considered when trying to design the converter: 1) The energy-storage capacitor voltage *V*bus should not be excessive. 1) The value of *V*bus should be kept to below. 800 V if possible so that the use of bulkier, more expensive capacitors can be avoided.

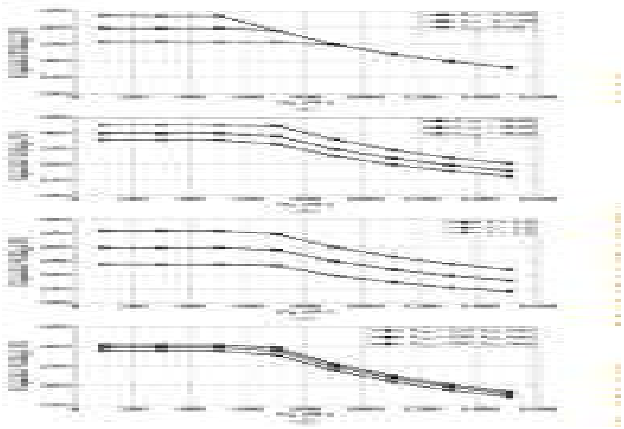


Figure7: Steady State Characteristic Curves (*Vin* = 208 *Vrms*, *Vo* = 48 V, *Fsw* = 50 Khz). (A) Effect of Output Inductor Value *Lo* On Dc Bus Voltage. (B) Effect of Input Inductor Value *Lin* on Dc Bus Voltage. (C) Effect of Transformer Ratio Value N on Dc Bus Voltage. (D) Effect of Input Voltage *Vin* on Dc Bus Voltage

1) Excessive peak output and input currents should be avoided if possible.
2) The input line current must satisfy the necessary regulatory agency requirements of harmonic content such as IEC1000-3-2 Class A. can be designed. The converter is to be designed with the following parameters for the example:

Input voltage : *V*in = 208 ± 10% *Vl*−*l*,rms

Output voltage : *Vrmo* = 48 V

Maximum output power : *Po* = 1500 W

Switching frequency : *fsw* = 1/*Tsw* = 50 kHz

Maximum capacitor voltage : (for each capacitor)450 V Input current harmonics : *EN*61000 − 3 − 2for Class A electrical equipment.

Discharge the bus capacitors. If *N* is high, the primary current may be too high and thus more conduction losses. *N* should be high enough to reduce the circulating primary current, then the primary current that is available to discharge the dc-link capacitors may be low and thus *V*bus may become excessive under certain operating conditions (i.e., high line). Equation (10) shows the relation between *V*bus, D, *Vo* and N. The minimum value of *N* can be found by considering the case when the converter must operate with minimum input line and, thus, minimum primary side dc bus voltage *V*bus,min and maximum duty cycle *D*max.

If the converter can produce the required output voltage and can operate with discontinuous input and continuous output currents in this case, then it can do so for all cases

$$N \geq \frac{v_{bus,min}}{2v_o} . D_{max} \ldots\ldots\ldots\ldots \quad \ldots\ldots(19)$$

Finding the proper value of *N* can be done with a computer program. As described in Section III, *V*bus is determined by the converter parameters for various values of *L*in and with fixed values of N. it should be the highest value for which valid operating points exist for the two most extreme line and load conditions: high line, light load and low line, full load. *N* has been chosen to be 3 for given example.

With a value of *N* = 3, *Vo* = 48, and *D*max = 0.75 the actual value of *V*bus can now be determined by using computer program which gives *V*bus,min = 384 V.

Step 2—Determine Value for Input Inductor Lin: The value for *L*in should be low enough to ensure that the input current is fully discontinuous under all operating conditions, but not so low as to result in excessively high peak currents. This can be done using the computer program with the following equations, which are based on the descriptions given in Section III.

For the case where *L*in is such that the input current remains discontinuous for all operating conditions, then the average input power can be expressed as

$$P_{in} = \frac{3}{\frac{\pi}{2}} * \left(\frac{1}{T_{su}} \int_0^{T_{su}} \left| v_{s,k} \right| i_{s,k} d_{w_k} t \right)$$

$$= \frac{3}{\frac{\pi}{2}} . \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} \left| v_{s,k} \right| i_{s,k} \ldots\ldots \quad \ldots..(20)$$

Where *fsu* is the input ac frequency and *fsn* = 2*fsw*/*fsu* and

$$i_{s,k} = \left(\frac{D+\Delta_s}{2} \right) i_{L_{in,max}}$$

$$= \frac{1}{4} \cdot \frac{D^2}{L_{in} f_{sw}} \cdot \frac{|v_{s,k}|}{1-\frac{|v_{s,k}|}{v_{bus}}} \ldots \ldots\ldots \quad ..(21)$$

By substituting the value of *is,k*(21), *P*in can be expressed as

$$P_{in} = \frac{3}{\frac{\pi}{2}} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} |v_{s,k}| i_{s,k}$$

$$= \frac{3.D^2}{8.\frac{\pi}{2}.L_{in}.f_{sw}} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} \frac{|v_{s,k}|^2}{1-\frac{|v_{s,k}|}{v_{bus}}} \ldots \quad ..22$$

By assuming the *P*in = *Po*, *L*in can be achieved

$$L_{in} = \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} |v_{s,k}| i_{s,k}$$

$$= \frac{D_2}{4.\pi P_o.f_{sw}} \cdot \frac{1}{f_{sn}} \sum_{k=0}^{f_{sn}-1} \frac{|v_{s,k}|^2}{1-\frac{|v_{s,k}|}{v_{bus}}} \ldots\ldots \quad \ldots.(23)$$

The worst case to be considered is the case when the converter operates with minimum input voltage and maximum load since if the input current is discontinuous under these conditions, it will be discontinuous for all other operating conditions, and thus an excellent power factor will be achieved. In this case, *V*in = 188 *V*phase,rms and *V*bus = 384 V as calculated in Step 1 are used to determine *L*in at the boundary condition for the input section, and *D* = *D*max = 0.75; assuming the converter to be lossless, *P*in = *Po* = 1500Wis used. The value of *L*in = 68 μH is found from the computer program. For this design, Lin = 65 μH is used.

Step 3: Determine Value for Output Inductor Lo

The output inductor can be designed in such a way that the output current to be in DCM or CCM or semicontinuous mode (SCCM). Therefore, there are three options to design output inductor.

1) The maximum value of *Lo* should be the value of *Lo* with which the converter's output current will be on the boundary between being continuous and discontinuous when the converter is operating with minimum input voltage, maximum duty cycle (*D*max), and full load (*Po,* max). If this condition is met, then the output current will be dis continuous for all other converter's operating conditions. The maximum value of *Lo* can therefore be determined to be

$$L_{o,max} = \frac{{v_o}^2}{P_{o,max}} \cdot \frac{(1-D_{max})}{2} \cdot \frac{T_{sw}}{2} \ldots \quad \ldots(24)$$

This results in a very high output ripple so that secondary diodes with high peak current ratings and large output capacitors to filter the ripple are needed.

2) ***Output Inductor for Full Output CCM:*** For having CCM at output, the minimum value of *Lo* should be the value of *Lo* with which the converter's output current will be continuous on the when the converter is operating with maximum input voltage, minimum duty cycle (*D*min), and minimum load (10% of *Po,*max). If this condition is met, then the output current will be continuous for all other converter's operating conditions. The minimum value of *Lo* can therefore be determined to be

$$L_{o,min} \geq \frac{{v_o}^2}{0.1 \cdot P_{o,max}} \cdot \frac{(1-D_{min})}{2} \cdot \frac{T_{sw}}{2} \ldots \quad .(25)$$

This results in a low ripple at output and low peak current rating for secondary diodes, and consequently lower output capacitor needs to filter the ripple. However, it has a major drawback. Bus voltage *V*bus is dependent on the current that is flowing in and out of the bus capacitor, which is, in turn, dependent on the output inductor currents. When the output current is CCM, then the dc bus voltage is dependent on the load, and it is not constant. This results in a high dc bus voltage at light load condition which needs to use high voltage dc bus capacitor and switches with higher rating. There are two solutions for this problem.

a) DC Bus Voltage Control by Changing Auxiliary Winding Turns Ratio

The auxiliary winding turns ratio can be designed in a way that does not completely cancel out the voltage across the dc bus capacitor. This reduces the amount of voltage placed across the input inductor and thus reduces the amount of energy pumped into the input inductor. Consequently, the reduced energy in the input inductor affects the energy equilibrium of the dc bus capacitor and thus reduces the dc bus voltage.

Reducing the number of auxiliary winding turns introduces dead band regions in the zero-crossing sections of the input current waveform. This is because the diode-bridge diodes are reverse biased when the input voltage is low, and current is not allowed to flow in the input inductor as the dc bus voltage is not fully cancelled out by the auxiliary winding [26]. Therefore, there is a trade off between the input pf and the dc bus voltage

reduction [27]. The auxiliary winding turns ratio should be selected to satisfy both the IEC1000-3-2 standards and reduce the dc bus voltage. For example, if choose *N*aux = 1.7 instead of 2, the bus voltage decreases 50 V. Figure 8 shows the variation of power factor versus variation of auxiliary winding turns ratio.

b) Output Inductor for Semi-CCM

This method is a compromising solution to have a continuous current at output for almost loads in one hand and preventing high dc bus voltage on the other hand. The output inductor should be designed so that the output current is made to be continuous under most operating conditions. The minimum value of *Lo* should be the value of *Lo* with which the converter's output current will be continuous on the when the converter is operating with maximum input voltage, minimum duty cycle (*D*min), and at least 50% of maximum load. The minimum value of *Lo* can therefore be determined to be

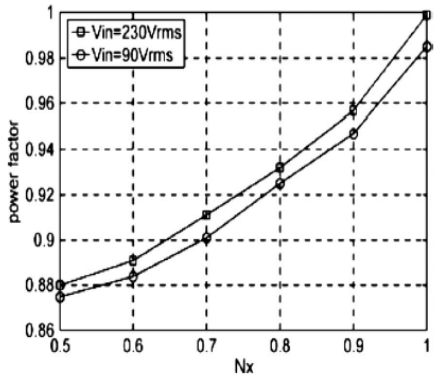


Figure 8: Variation of Pf for Different Values of Auxiliary Winding Turns Ratio [26]

$$L_{o,min} \geq \frac{{v_o}^2}{0.5 \cdot P_{o,max}} \cdot \frac{(1-D_m)}{2} \cdot \frac{T_{sw}}{2} \ldots \quad \ldots(26)$$

In this paper, SCCM mode for the output current is assumed. Substituting *Po*,max = 1500 W, *Vo* = 48 V, *Tsw* = 20 μs, and *Dm* = 0.5 gives *Lo*,min = 7 μH and the value of *Lo* should be larger to provide some margin. The value of *Lo* should be larger to provide some margin. On the other hand, according to Figure 7(a), the value of *Lo* cannot be too high as the dc bus voltage of the converter will become excessive; a value of

Lo = 11 μH is chosen

VI. EXPERIMENTAL RESULTS

An experimental prototype of the proposed converter was built to confirm its feasibility. The prototype was designed according to the following specifications:

Input voltage *V*in = 208 ± 10% Vrms (line-line)

Output voltage *Vo* = 48 V

Output power *Po* = 1.5 KW

Switching frequency *fsw* = 50 kHz.

The main switches are FDL100N50F, and diodes are UF1006DICT. The input inductors are *Labc* = *L*in = 60 μH, the dc link capacitors are *C*1, *C*2 = 2200 μF, and the output inductor is *Lo* = 11 μH. The auxiliary transformer ratio is 1: 2, and the main transformer ratio is 3 : 1. Typical converter waveforms are shown in Figure 9–11 for different loads. It can be seen that the proposed converter can operate with no dead band regions, that it is a multilevel full-bridge converter, that the switch stress is half the dc bus voltage, and that it can operate with a continuous output current, unlike most other converters of the same type. The lack of dead band regions in the input current waveforms is due to the greater flexibility that is allowed by the proposed converter's multilevel structure—there is less need to distort the input current to try to prevent the dc bus voltage from becoming excessive. It should be noted that, like other previously proposed converters with discontinuous input currents, the high input current ripple is a source of EMI. Suggestions for dealing with EMI issues in these converters can be found in [28]. Figure 12 shows the efficiency of the converter at different values of the output power. Figures 13 and 14 show the input current harmonics a *Po* = 1500 W and *Po* = 750 W when *Po* = 1500 W when *V*in = 220 *Vl*−*l*rms. It can be seen that the converter's harmonics are below the harmonic levels that are specified by the IEC 1000-3-2 standard.

The efficiency measured from the converter at light load was about 93% and for full load was 91% as shown in Figure 10. In multilevel converters such as the proposed converter, the voltage stresses of their power switches are only half of the input voltage and not the full input voltage as is the case for two-level converters. This means that less energy is required to discharge the output capacitances of switch MOSFET devices, and thus they can operate with fewer switching losses and a wider load range for zero-voltage switching (ZVS) than two level converters. Compared to other multilevel converters such as the ones proposed in [17] and [22], the proposed converter is simpler (in terms of topology and in capacitor voltage balancing), has better lighter load efficiency (since its switches are exposed to less voltage and thus it is easier to discharge switch capacitances during switch turn-on with less primary current), and can operate with less output inductor current ripple, even continuous output inductor current at heavier loads. In terms of total harmonic distortion

(THD), the proposed converter has low THD, less than 7%, which is similar to the converters in [17] and [22].

VII. CONCLUSIONS

The proposed converter has the following features.

- Proposed converter has an auxiliary circuit that can cancel the capacitor voltage in which way the input inductor acts as a boost inductor to have a single-stage PFC.
- Proposed converter can operate with lower peak voltage stresses across the switches and the dc bus capacitors as it is a three-level converter. This allows for greater flexibility in the design of the converter and ultimately improved performance.
- Proposed converter can operate with an input current harmonic content that meets the EN61000-3-2 Class A standard.
- Output inductor of the proposed converter can be designed to work in CCM mode over a wide range of load variation and input voltage. This results in a lower output inductor current ripple than that found in other two-level single stage converter, which ultimately results in lower peak current stresses for the secondary components.

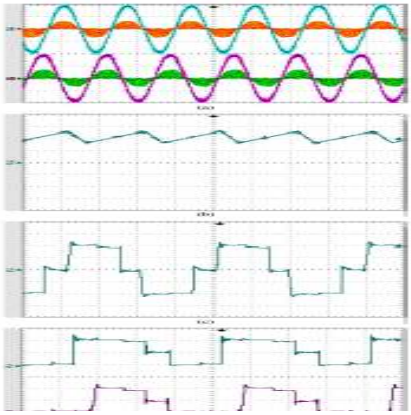


Figure 9: Experimental Results (A) Input Current and Voltage (For Two Phases) (V: 100 V/Div, I: 15 A/Div). (B) Output Inductor Current (I: 15 A/Div., *T* : 5 *M*s/Div.). (C) Primary Voltage of the Main Transformer (V: 150 V/Div., *T:* 5 *M*s/Div). (D) Bottom Switch Voltages *V*ds4 and *V*ds3 (V: 150 V/Div, *T:* 5 *M*s/Div)

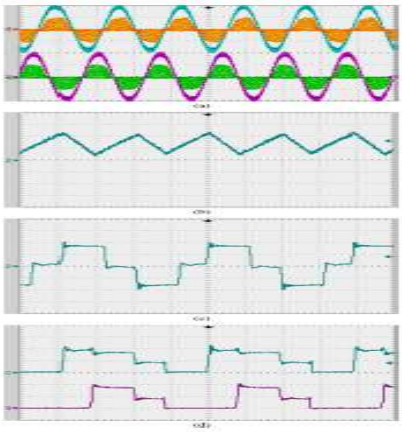


Figure 10: Experimental Results For 50% of Full Load. (A) Input Current and Voltage (For Two Phases) (V: 100 V/Div, I: 10 A/Div). (B) Output Inductor Current (I:15 A/Div., *T* : 5 *M*s/Div.). (C) Primary Voltage of the Main Transformer (V: 200 V/Div., *T* : 5 *M*s/Div.). (D) Bottom Switch Voltages *V*ds4 And *V*ds3 (V: 200 V/Div., *T* : 5 *M*s/Div.)

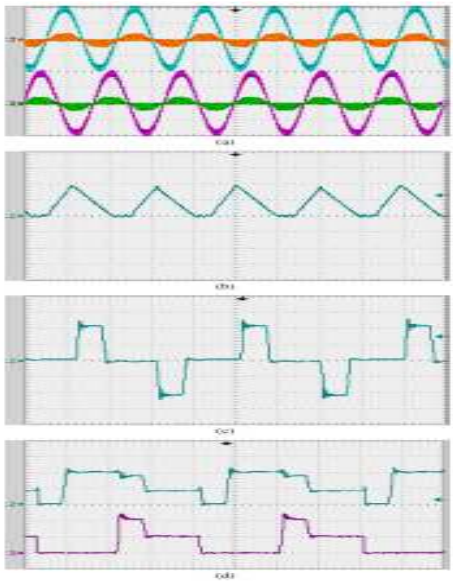


Figure 11: Experimental Results For 25% of Full Load. (A) Input Current and Voltage (For Two Phases) (V: 100 V/Div, I: 10 A/Div). (B) Output Inductor Current (I: 10 A/Div., *T:* 5*μ*s/Div.). (C) Primary Voltage Of The Main Transformer (V: 200 V/Div., *T* : 5 *M*s/Div.). (D) Bottom Switch Voltages *V*ds4 and *V*ds3 (V: 200 V/Div., *T:* 5 *M*s/Div)

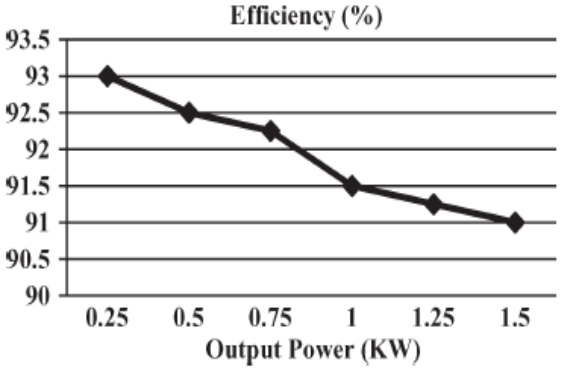


Figure 12: Converter Efficiency with Input Voltage *VLL*−rms = 220 V

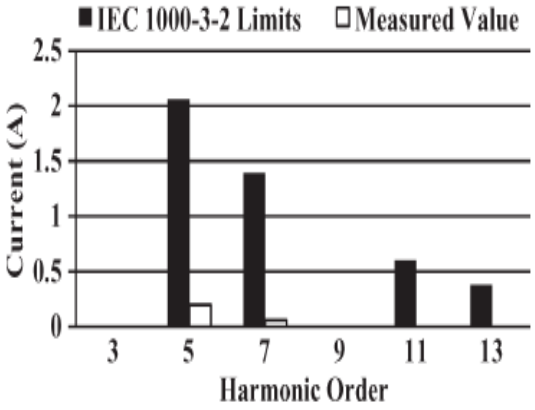


Figure 13: Input Current Harmonic at *V*in = 220 *V*rms(*l* − *l*), *Po* = 1.5 KW Compared to IEC1000-3-2 Class A Standard Figure

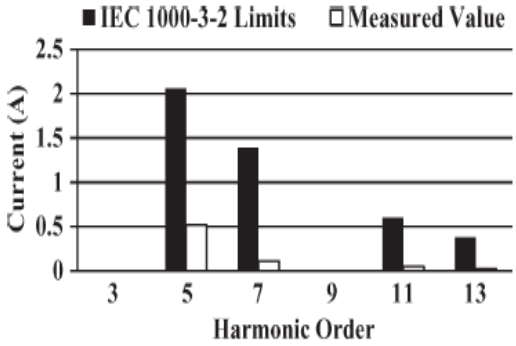


Figure14: Input current harmonic at *Vin* = 220 *Vrms*(*l* − *l*), *Po* = 0.75 KW compared to IEC1000-3-2 Class A standard

- Converter is simple and can be implemented with a simple passive auxiliary circuit to balance the dc bus capacitor voltages.

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